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(71) Applicant: **NOKIA MOBILE PHONES LTD.**
P.O. Box 86
SF-24101 Salo(FI)

(72) Inventor: **Leppänen, Pentti, Oulun yliopisto**
Tietotliikennelaboratorio,
Linnanmaa X2
SF-90570 Oulu(FI)
Inventor: **Iinatti, Jari, Oulun yliopisto**
Tietotliikennelaboratorio,
Linnanmaa X2
SF-90570 Oulu(FI)

(74) Representative: **Frain, Timothy John**
Patent Department
Nokia Mobile Phones
Ashwood House
Pembroke Broadway
Camberley, Surrey GU15 3SP (GB)

(54) Receiver using a matched filter and a median filter.

(57) A circuit arrangement for reducing the adverse effects of interference on a signal using a matched filter. The circuit arrangement comprises a matched filter (7) and a median filter (9). The median filtered output signal of the matched filter is utilized to remove interference, to calculate the threshold level, or to estimate the interference level at the output of the matched filter.

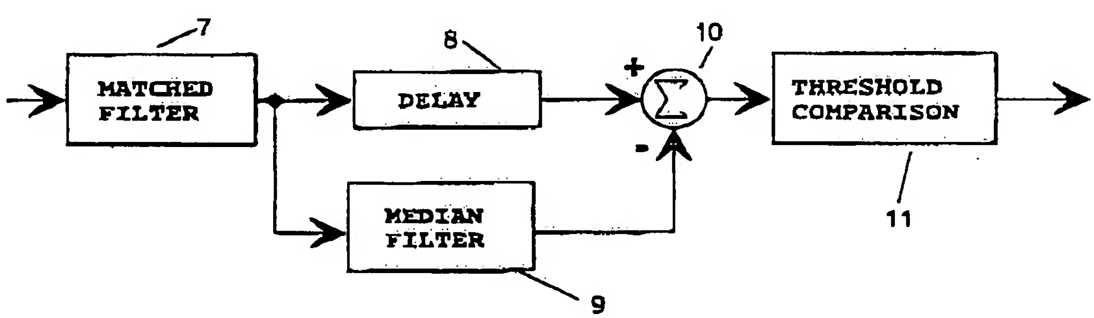

FIG. 5

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The present invention relates to a circuit arrangement for reducing the adverse effects of an interference signal on a data signal.

The term data signal is intended to mean any signal carrying data or information, including telecommunications data.

A matched filter is used to detect a signal e.g. in telecommunications. The impulse response of a realizable matched filter is a signal, which is scaled, delayed and inverted in time. At the output of the filter matched to the signal we obtain the maximum level when the signal is completely received.

The output waveform of the filter is proportional to the autocorrelation function of the signal itself. In an Additive Gaussian White Noise (AGWN) channel the matched filter maximizes the momentary signal to noise ratio and minimizes the error probability of the transmission system. If also interference is added to the signal in the transmission channel the receiver will not anymore operate in an optimal way, and the performance will be reduced.

A matched filter is also used in distributed spectrum telecommunication systems. Then it can be used for the detection of a data signal and also i.e. in the search phase for the code synchronization of the receiver, so that the filter impulse response is a time inverted, scaled and delayed version of the distribution code or part of it.

The prior art is described below with reference to Figures 1 to 3 of the accompanying drawings, in which:

Figure 1 shows a code synchronization system, selected as an example, in accordance with the prior art;

Figure 2 shows the output signal of the prior art matched filter in Figure 1; and

Figure 3 shows the signal provided by the threshold comparison block.

Figure 1 shows a prior art code synchronization system. The code synchronization system comprises a filter 1 matched to the distribution code, a threshold comparison means 2, and means 3 for activation of the monitoring.

The maximum value is obtained at the filter 1 output when the distribution code or a part of it is received, and it can synchronize the code generator or the receiver after the threshold comparison.

Figure 2 shows the output signal of a prior art matched filter in an exemplary case. The exemplary case is ideal and the code contains L chips and the chip period is T seconds. The output signal 4 is now an ideal autocorrelation function containing impulses having a height of L times the level of the received signal, the repeating period being the code length L x T seconds.

Figure 3 shows the signal provided by the threshold comparison block. The signal 5 of the threshold comparison block 2 has the value "1" when the output signal 4 of the matched filter exceeds the threshold level.

For example a deterministic error could be disastrous, because remnants of the interference could be evident at the output of the filter 1. Then the synchronization ability decreases, preferably if the code's autocorrelation function form is not ideal and contains side lobes, which in combination with the interference response could cause the threshold level to be exceeded. The matched filter 1 certainly attenuates the interference, but for instance the attenuation of a continuous interference at the average frequency of the filter decreases when the balance of the distribution code increases, or in a binary case, when the number of ones and zeroes increases.

Usually we try to remove the interference by different attenuation or correction algorithms. These methods are often complicated and require computing time in order to estimate the characteristics of the interference or the state of the channel.

According to the present invention there is provided a circuit arrangement for reducing the adverse effects of an interference signal on a data signal, the circuit arrangement comprising a matched filter characterized in that the output of the matched filter is coupled to a median filter to compensate for rapid changes in the data signal, and the output of the median filter is coupled to a calculation circuit in which a signal characteristic of the interference signal at the output of the matched filter is determined such that the data signal may be compensated for the efect of the interference signal.

An advantage of the present invention is the provision of a circuit arrangement which will address the above presented disadvantages and problems.

Embodiments of the present invention are described, by way of example, with reference to Figures 4 to 7 of the accompanying drawings, in which:

Figure 4 shows the median filtered output signal of the matched filter in principle;

Figure 5 shows the block diagram of a circuit arrangement, in accordance with the invention;

Figure 6 shows a block diagram of an alternative circuit arrangement, in accordance with the invention; and

Figure 7 shows the block diagram of another alternative circuit arrangement, in accordance with the invention.

It is well known that rapid changes or impulses can be removed from a signal with a median filter, which is illustrated in figure 4 where the output signal of a matched filter is fictitiously median filtered. In median filtering the signal or samples

taken of it are processed so that a median (MED) is calculated for each $2k+1$ samples, in which k is an integer. Then the output signal 6 of the median filter is

$$y(n) = MED\,[x(n-k), x(n-k+1), \ldots, x(n), \ldots, x(n+k)].$$

$x(n)$ is an input signal, in which the integer n represents the sampling moment as multiples of the sampling interval.

The solution in accordance with the invention presents a different circuit arrangement to estimate and to remove the interference with the aid of a median filter. An advantage of the circuit arrangement in accordance with the invention is based on the impulse nature of the output signal of the matched filter.

Figure 5 shows a block diagram of an embodiment of the circuit arrangement in accordance with the invention. The circuit arrangement comprises a filter 7 matched to the signal, a delay element 8, a median filter 9 and an adder 10, followed by a threshold comparison 11. In a traditional case samples are taken at the output of the matched filter 7, and they are compared to a threshold level in the threshold comparator 11, after which the presence of a signal is determined. Particularly, when there occurs a deterministic error it is possible that the base level of the samples between the impulse peaks exceeds the threshold, whereby erroneous decisions could be made continuously.

In the circuit arrangement the signal or the samples obtained from the matched filter 7 are median filtered in the median filter 9 so that the median of $2k+1$ samples is calculated

$$y(n) = MED\,[x(n-k), x(n-k+1), \ldots, x(n), \ldots, x(n+k)].$$

At the same time samples obtained at the output of the matched filter 7 are delayed by k samples in the delay means 8, after which the difference between the delayed signal and the sample sequence provided by the median filter 9 is calculated in the adding means 10. Only then the difference signal is compared with the threshold level in the comparison means 11.

Here the circuit arrangement has an advantage that the offset from the base level, caused by the interference, can be removed from the signal and at the same time we obtain information about the interference. The median filter 9 is basically of a low-pass type. The calculation of the difference signal corresponds to a high-pass type processing in order to remove the interference, the processing being based on the impulse-like nature of the actual useful signal.

Figure 6 shows the block diagram of an alternative solution of the circuit arrangement in accordance with the invention. In the alternative circuit arrangement the signal or the samples obtained from the filter 7 are median filtered in the median filter 9 so that the median of $2k+1$ samples is calculated. At the same time the samples obtained at the output of the matched filter 7 are delayed by k samples in the delay means 8, after which the delayed signal is supplied to the decision circuit 13. In the decision circle 13 the output signal is determined on the basis of the basic data.

Figure 7 shows the block diagram of another alternative solution of the circuit arrangement in accordance with the invention. In the second alternative solution the signal or samples obtained from the matched filter 7 are median filtered in the median filter 9 so that the median of $2k+1$ samples is calculated. The obtained signal is supplied to the calculation circuit 14, which calculates the output signal.

In view of the foregoing it will be clear to a person skilled in the art that modifications may be incorporated without departing from the scope of the present invention.

Claims

1. A circuit arrangement for reducing the adverse effects of an interference signal on a data signal, the circuit arrangement comprising a matched filter characterized in that the output of the matched filter is coupled to a median filter to compensate for rapid changes in the data signal, and the output of the median filter is coupled to a calculation circuit in which a signal characteristic of the interference signal at the output of the matched filter is determined such that the data signal may be compensated for the effect of the interference signal.

2. A circuit arrangement as claimed in claim 1, wherein the output of the matched filter is additionally coupled to the calculation circuit via a second circuit comprising a delay means.

3. A circuit arrangement as claimed in claim 2, wherein the delay means delays the output signal from the matched filter by "k" samples prior to being supplied to the calculation circuit.

4. A circuit arrangement as claimed in claim 2 or 3, wherein the difference between the output of the delay means, and the output of the matched filter is calculated in the calculation circuit to provide a signal characteristic of the interference signal.

5. A circuit arrangement as claimed in any of claims 2 to 4, wherein the circuit arrangement comprises an adder (10), whose positive input receives the output of the matched filter (7) through a delay means (8), and whose negative input received the output of the matched filter (7) through a median filter.

6. A circuit arrangement as claimed in any of claims 2 to 5, wherein the signal or samples obtained from the matched filter are filtered in the median filter so that a median of 2k+1 samples is calculated and that at substantially the same time the samples obtained at the output of the matched filter are delayed by k samples in the delay means.

7. A circuit arrangement as claimed in any of claims 2 to 6, wherein the delayed signal is supplied to the decision circuit, the difference provided by the median filter is supplied to the calculation circuit, which calculates a threshold value and then supplies it to the decision circuit, which determines the output signal

8. A circuit arrangement as claimed in any of the previous claims, wherein the signal or the samples obtained from the matched filter are filtered in the median filter so that a median of 2k+1 samples is calculated, and that the obtained signal is supplied to the calculation circuit, which calculates the output signal.

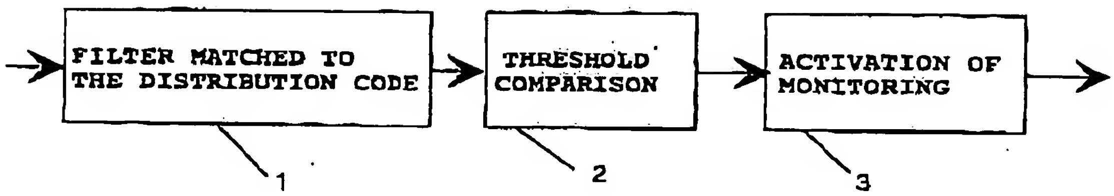

FIG. 1

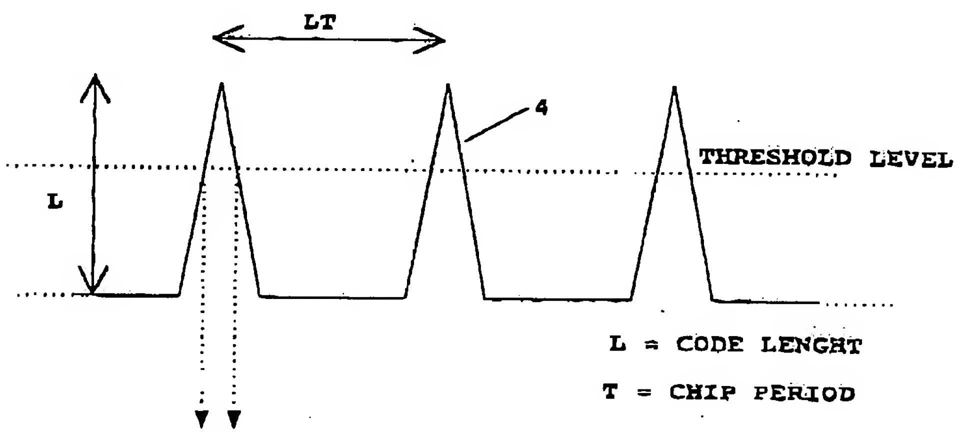

FIG. 2

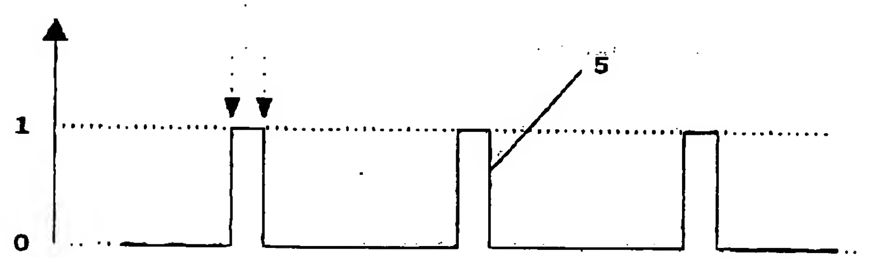

FIG. 3

FIG. 4

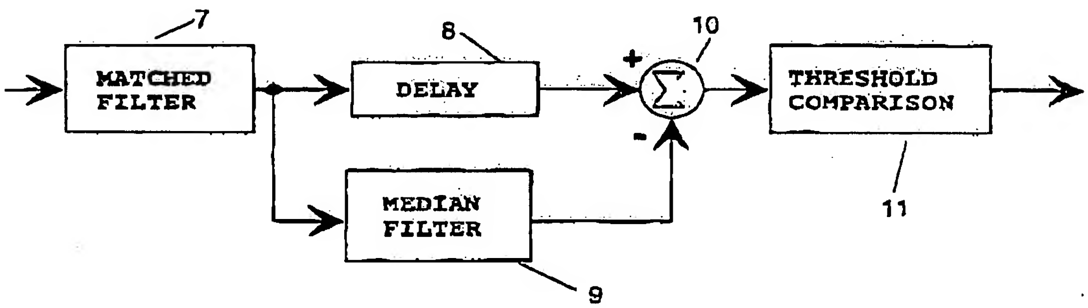

FIG. 5

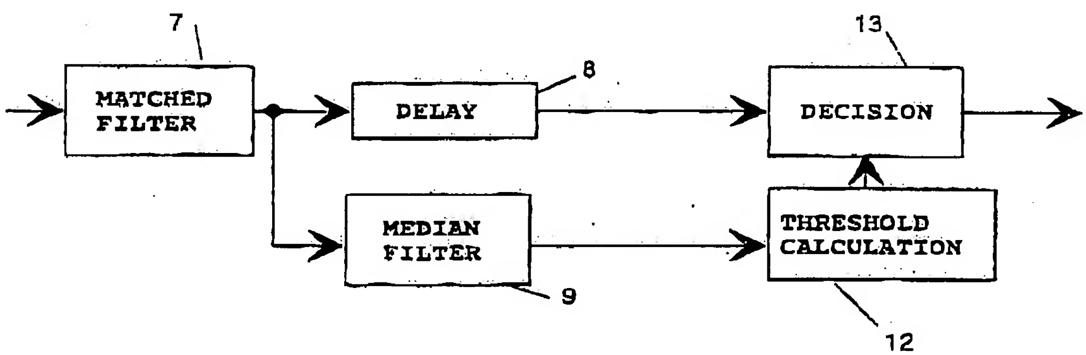

FIG. 6

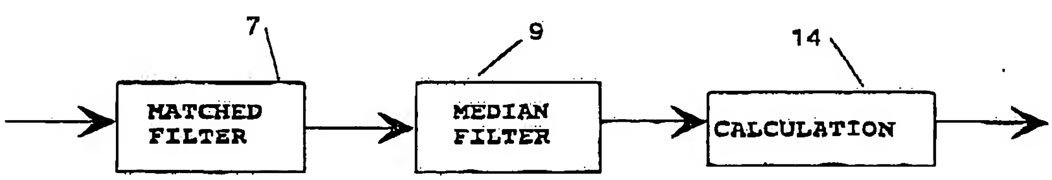

FIG. 7

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EUROPEAN SEARCH REPORT

Application Number
EP 93 30 5141

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
Y	IEEE TRANSACTIONS ON COMMUNICATION TECHNOLOGY vol. COM-19, no. 6 , December 1971 , NEW YORK US pages 1163 - 1172 CAHN 'Performance of Digital Matched Filter Correlator with Unknown Interference'	1,2	H04J13/00
A	* page 167, line 2 - line 6; figure 3 * * page 1163, right column, line 1 - page 1164, left column, line 6; figure 1 *	3-8	
Y	DE-A-39 22 972 (CLARION CO. LTD.) * column 1, line 68 - column 2, line 8; figure 1 * * abstract *	1,2	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)
H04B
H04J
H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	8 December 1993	Bossen, M

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